

1 What is claimed is:

2 1. A gain control circuit in a radio frequency transmission path for an amplifier stage
3 adjacent and an antenna and having an input terminal, an output terminal and first and
4 second control terminals comprising:

5 a fixed resistance connected between said input terminal and said output terminal;
6 a first semiconductive circuit connected between said fixed resistance at a level of
7 reference potential and second semiconductive circuit connected across said fixed
8 resistance a control terminal of said first semiconductive circuit for connection to a gain
9 control signal for decreasing resistance of ³⁶said semiconductive circuit in response to
10 increase of the radio frequency signal, and a control terminal of the second semi-
11 conductive circuit connected to complimentary gain control signal for having its
12 resistance raised and increasing impedance of said gain control circuit in correspondence
13 with a decrease of impedance said first semiconductive circuit

1 2. The gain circuit of claim 1 where an said first and second semi-conductive
2 circuits comprise source-drain circuits of first and second CMOS transistors respectively,
3 and (said control electrode) of each said semiconductive circuit comprises a gate electrode.

1 3. The circuit according to claim 2 wherein said resistance comprises first and
2 second resistors and said first semiconductive circuit is connected to a terminal
3 intermediate said first and second resistors.

1 4 The circuit of claim 3 wherein said first and second resistors are of equal value.

1 5. An output signal path and a transmitter comprising a gain control circuit
2 according to claim 4, a Gilbert Cell modulator output connected to the input terminal of said
3 gain control circuit and a final stage power amplifier coupled between said output
4 terminal of said gain control circuit and an antenna.

1 6. A receiver input circuit comprising a gain circuit according to claim 4, an input
2 fixed amplifier coupled between an antenna and said input terminal and said gain circuit

3 and an amplifier connected between said output terminal of said gain circuit and an input
4 to a demodulation stage.

1 7. In a direct conversion ~~wireless communication transceiver~~ having an input stage
2 and an output stage, said input and output stages respectively comprising amplifiers
3 adjacent an antenna, the improvement wherein said receiver comprises a fixed gain input
4 amplifier coupled to a gain circuit according to claim 4.

1 8. The improvement according to claim 7 wherein said output stage comprises a
2 fixed gain amplifier coupled to an antenna and a gain circuit according to claim 4
3 providing an input to said power amplifier.

1 9. In a direct conversion transceiver comprising an input stage and an output stage
2 the improvement wherein said output stage comprises a fixed power amplifier connected
3 to coupled to an antenna and a gain circuit according to claim 4 in providing an input in
4 to said power amplifier circuit.

1 10. A method for ~~controlling gain~~ and providing a ~~constant impedance~~ in a signal
2 path comprising the steps of measuring a ~~radio frequency~~ signal to produce a gain control
3 signal;

4 proportioning said gain control signal into first and second components, to
5 provide first and second gain control signals;

6 ~~adjusting gain of said circuit~~ ^{N/A} in accordance with said first control signal;
7 and changing ~~the impedance~~ ^{DOS} of said circuit in accordance with impedance change
8 provided by said gain adjustment.

1 11. The method of claim 10 comprising providing first and second fixed resistances
2 connected between an input terminal and an output terminal of the gain control circuit,
3 wherein the step of adjusting gain comprises varying conductivity of a source-drain
4 circuit connected between a terminal intermediate said first and second resistors end
5 ground inversely with magnitude of the measured radio frequency signal, wherein the
6 step of adjusting impedance comprising increasing resistance of a source-drain circuit
7 connected across the first and second resistors.

GOVERNMENT PROPERTY